

ESD Station Model 1200 Series

1200 E : HBM/MM Pin Combination ESD Tester

1200 EL : HBM/MM Pin Combination ESD /Latch-up Tester

1200 ELC: HBM/MM Pin Combination ESD/Latch-up and CDM Tester





Features

- 4 functions; HBM, MM, Latch-up and CDM in one system
- Maximum 1350 pins test available (Between non-supply pin and supply pins using special DUT Board)
- Every Device level ESD test including CDM test available

Applications

- Device development evaluation
- Quality Assurance
- Device qualification and incoming test
- device handling

ESD Test

- Meets variable Standards
- •Full pin combination
- 3 Modes of charge removalDamage progress viewable
- Plentiful damage detection

CDM Test

- Meets international standards
- Automated test
- Direct Charging or FI-CDM
- Repeatable and stable discharge waveform.

Latch-up Test

- Meets international standards
- Stabilizing I_{CC} current
- ●High Speed test by Successive approximation
- ●High Temp test up to 125°C

General descriptions:

The ESD Station Model 1200 ELC tester is the world's FIRST commercially available ESD Test System that combines all ESD, Latch-Up and CDM tests in ONE system – for devices up to 256 pins. If a dedicated DUT Board is provided (as the DUT Board example 2 on the next page), non-supply pin vs. supply pin ESD Test up to 1350 pin pairs can be tested automatically, though this is some sort of a simplified ESD test.

This system can include 128 or 256 pins full pin-combination ESD test function as well as up to 4 Vcc supply Latch-up test capability and with CDM test that meets JEDEC standard with options to meet ESDA or JEITA standards.

Model 1200E : Supports HBM and MM ESD tests.

Model 1200EL : Supports HBM, MM and Latch-up tests.

Model 1200ELC: Supports HBM, MM, Latch-up and CDM tests.

By the ESD test, relations between device damage and ESD stress can be tested. The ESD stress includes Human Body Model (HBM) and Machine Model (MM). The model 1200E includes both HBM and MM but other stress model may be easily included as options. Any 128 or 256 pins can be programmed as ESD return pins (Terminal B) so that full pin combination test required by many ESD standards is allowed.

Latch-up test measures the latch-up sensitivity of the CMOS devices detecting the latch-up current (Idd at latch-up detected). Current pulse, voltage pulse and supply over voltage pulse are included in the basic system as the trigger source of Latch-up. Also, HBM and MM ESD pulse may be used to trigger latch-up if required. Other latch-up trigger source can be installed as the option so that transient latch-up can be evaluated. To get a stable latch-up test result, it is very important to stabilize the device internal conditions as well as supply current, I_{CC}. The pull-up/down functions for all pins are provided by the basic configuration for this purpose. Clock and pattern generation is provided as an option as well.

Basic configuration of CDM tester, model 1200ELC, will include JEDEC air discharge CDM head that stimulates Field Induced CDM (FI-CDM or F-CDM). Optionally, other CDM head can be provided such as DI-CDM (or D-CDM for JEITA standard) as well as FI-CDM for ESDA or AEC standard. All CDM models simulate the fast air discharge stress caused by the charged device metal terminal contact to the external metal.



Model 1100E (High Pin count ESD Tester without supporting Pin Combination Test)



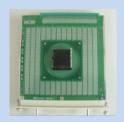
Inner view of the ESD Test Fixture



MM ESD Pulse Generator (EPG) Unit

ESD test

Main window of ESD % method test ESD pulse voltage, polarity, period, repetition, pin combination and others are programmed by this window. I-V curve measurement points, averaging number and test pins will be defined as well.



DUT Board example 1 For pin combination

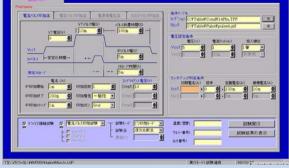


DUT Board example 2
For Higher pin count

Latch-up Test

Main Window of Current pulse triggered Latch-up test

Pulse width, period, current values, Vcc voltage and latch-up current criteria are programmed.



ESD Test condition programming Window

Current latch-up test programming Window

CDM Test

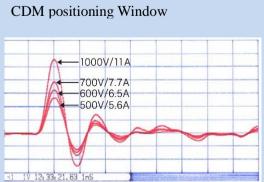
Right Window for CDM positioning Even to the fine contact pitch devices such as 0.4mm, CCD camera and Monitor view and capacitance measurement system will allow easy and reliable positioning. These features will work during test as well as programming the DUT pin positioning.



CDM Discharge Waveform

Right picture shows discharging waveform from the small capacitance module.

F-CDM requests air discharge except AEC, and it is variable depending on humidity, contact contamination and other environments. Model 1200ELC will give you a reasonable solution to it using relay discharge as well.



Small module discharge waveform, 6.8pF

Specifications

(ESD Test Specifications)

Test Items including options

V-I Curve measurements

ESD Simulation

ESD test using V-I curve % variation

V-I curve graph display

ESD Part

Stress voltage

HBM: $\pm 5V$ to 4000V/5V MM: $\pm 5V$ to 2000V/5V

 $HBM: \pm 8000V(Option)$

Voltage accuracy: $\pm 5\% + 5V$ of programmed value

Pin selection: 2 axis robot ESD Repetition: 1 to 100

ESD Period: 300ms to 5s in 100ms step

Charge removal mode: 3 mode by program selection Standards: MIL, JEDEC, JEITA, ESDA, AEC

●Source meter (VF/IM)

Voltage source (VF)

 ± 10 mV to ± 50 V, 3 digits Accuracy: $2\% \pm 20$ mV

Measured current (IM)

 ± 10 nA to ± 100 mA, Accuracy: $2\% \pm 20$ nA

■Test Pin Count

128 pins or 256 pins (As the Full Pin Combination System) 1350 pins (At only non-supply pin vs. Supply pins test using a dedicated DUT board)

[CDM Test Specifications]

Models: D-CDM and/or F-CDM

Standards: JEITA, JEDEC, ESDA, AEC

Pin count: Max2048/Device # of DUT: Max10DUT/Jig Positioning accuracy: ±0.05mm

Package: DIP, QFP, SOP, TAB, BGA and others

Positioning method: CCD Camera, Capacitance sensor,

Current peak detection

[LATCH-UP Test Specification]

Test Items

Current Pulse Latch-up Test Voltage Pulse Latch-up Test Supply Overvoltage Latch-up Test ESD Pulse Latch-up Test

Pulse Generator

Current Range: 1mA to 1000mA/1mA step (0 - 20V)

1mA to 100mA/1mA step (20 - 50V)

Voltage Range: 50mV to 20V (1A)

20V to 50V (100mA)

Pulse width: 1ms to 100ms (1ms step)

Repetition: 1 to 100

Supply overvoltage pulse: 0 to 20V (1A)

: 20V to 50V (100mA)

● Latch-up detection power supply Vcc1 to 4

Test Voltage: $\pm 50V/50mV$

Iccq test current: DC 0 - 0.5A (100nA Resolution) Latch-up detection current: 0 - 1A (1mA Resolution)

Any Vcc supply can be combined with the above pulse generator so that supply overvoltage test to any supply channel can be done.

•max HI/min LO Supply (Only for Latch-up test)

of Channel: 3

Voltage: $0 - \pm 15V$ (0.1V Step)

●Clock/Pattern Generator (Optional)

4 clock Channels: 1us~100us/1us step

16 channels pattern + Sync clock depth: 1024

H/L Levels: H=2 - 15V, L=0V

Test Pin Count

128pins or 256 pins

Other specifications

Operation Temperature: 15°C-40°C Humidity: less than 60%

AC Power:100V±10%, 50/60Hz, 1Phase, 800VA

Other AC Voltage optionally available

Host Controller: PC(Windows-7) and LCD Monitor

Safety: EPO, Interlock, Leakage Breaker

Main body size and weight: About $570W \times 860D \times 570H(mm)$

excluding a signal tower, About 60kg

Sub cabinet size and weight: About 570W \times 890D \times

830H(mm), About 100kg*1

PC table : About $800W \times 800D \times 1400H(mm)^{*2}$

Size and weight of a DUT Board case: About 340W \times 360D \times

560H(mm) and 6kg.

*¹If more than one Latch-up detection power supply is ordered, sub cabinet weight will be increased 8kg/# of supply.

*2We recommend PC table is purchased locally to save freight charge for over sea installation because the price of the PC table may be lower than the air freight of it.

Specifications are subject to change without notice. Please confirm the latest specifications before placing the order.

Contact: